REMARKS

Claims 1 through 20 remain pending in this application. In response to the Office Action dated July 10, 2003, this RCE and amendment is submitted. Claim 1 has been amended. Care has been taken to avoid the introduction of new matter. Favorable reconsideration of the application in light of the following comments is respectfully solicited.

Claims 17 through 20 stand allowed. Claims 1 through 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Lepejian, of record, the statement of rejection appearing in the Office Action of March 26, 2003. Claim 1 is the only rejected independent claim. In the response filed June 25, 2003, claim 1 was not amended, the rejection having been traversed for the reasons summarized below.

The select circuit of claim 1 switches between a signal applied from the ATE external to the memory device and a signal from the BIST circuit with a programmable ALPG in the device. The signal (from ATE or BIST circuit) applied to the select circuit is a command control signal to control the memory device or an address signal addressing a memory array, not the data written/read out with respect to the memory array. By virtue of this select circuit, the cost required for testing facilities such as ATE can be suppressed even if the storage capacity of the memory device is increased in a test mode by conducting a test using the internal BIST circuit. Also, since the BIST circuit connected by the select circuit is a programmable BIST circuit, a desired test pattern can be generated as the ATE even after the fabrication process (after the wafer process).

Lepejian teaches that a multiplexer is provided at the memory input/output line so that the data read out from the memory can be returned, when the memory is in a test mode,

to an adjacent bit in a subsequent writing operation. Multiplexer 45 in Lepejian device functions to switch so as to increment or decrement the sequence of the address generated by an address generation circuit 40, and is completely different from the select circuit of claim 1 in the present invention.

The Office Action of July 10, 2003 maintained the rejection, asserting that the features focused upon in the response are not recited in the rejected claims. Specifically, the Office Action holds that the claims do not require that "[t]he signal (from the ATE or BIST circuit) applied to select the circuit is a command control signal to control the memory device or an addressing array, not the data written/read out with respect to the memory array (emphasis in the Office Action." In response, independent claim 1 has been amended in the last paragraph to recite:

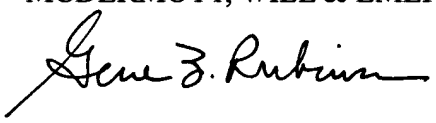
> a select circuit *applying to said memory cell array a command control signal* and an address signal for testing said memory cell array, selectively from either said built-in self test circuit or said input buffer test data applied from said test circuit and data applied from said input buffer according to whether in a test operation or a normal operation.

Lepejian, as discussed above, embodies a multiplexer that functions as a switch to increment or decrement the sequence of the address generated by an address generation circuit. Lepejian does not disclose or suggest selectively applying a command control signal to the memory cell array as now expressly recited in independent claim 1. As claim 1 can no longer merit the broad interpretation rendered in the Office Action, and since Lepejian does not disclose or suggest selective application of a command control signal as required by the claim, it is submitted that the application as amended overcomes the rejection of claim 1 and its dependent claims 2 through 16. Allowance of the application is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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